HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200209576-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Mei

Confirmation No.: 8740

Application No.: 10/769,127

Examiner: Tran, Thanh Y

Filing Date: January 30, 2004

Group Art Unit: 2822

Title: FORMING A SEMICONDUCTOR DEVICE

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on April 22, 2008

[X] The fee for filing this Appeal Brief is $510.00 (37 CFR 41.20)

[ ] No Additional Fee Required

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply

[ ] (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

[ ] 1st Month $120	[ ] 2nd Month $460	[ ] 3rd Month $1050	[ ] 4th Month $1640

[ ] The extension fee has already been filed in this application

[X] (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 510 . At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

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Date of facsimile: June 10, 2008

Typed Name: Wendell J. Jones

Signature:

Respectfully submitted,

Mei

By

Wendell J. Jones

Attorney/Agent for Applicant(s)

Reg. No. 45,961

Date June 10, 2008

Telephone (408) 938-0980

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Respectfully submitted,
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Page 1 of 2 (Appeal)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant:	Mei	Examiner: Tran, Thanh Y.
Serial No.:	10/769,127	Group Art Unit: 2822
Filed:	January 30, 2004	Docket No.: 200209576-1
Title:	FORMING A SEMICONDUCTOR DEVICE	

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on April 22, 2008, appealing the final rejection of claims 1, 3, 13, 14 and 17 of the above-identified application as set forth in the Final Office Action mailed March 13, 2008.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of $510.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. §41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1, 3, 13, 14 and 17.

06/11/2008 VBUI11 00000034 082025 10769127
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Appeal Brief to the Board of Patent Appeals and Interferences
Appellant: Mei
Serial No.: 10/769,127
Filed: January 30, 2004
Docket No.: 200209576-1
Title: FORMING A SEMICONDUCTOR DEVICE

TABLE OF CONTENTS

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed March 13, 2008, claims 1, 3, 13, 14 and 17 were finally rejected. Claims 11, 12, 21 and 24-30 were previously withdrawn. Claims 2, 4-10, 15-16, 18-20, and 22-23 were objected to. Claims 1-10, 13-20, 22 and 23 are pending in the application, and are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been entered subsequent to the Final Office Action mailed March 13, 2008. No Response After Final was filed.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The Summary is set forth as an exemplary embodiment as the language corresponding to independent claims 1 and 13. Discussions about elements of claims 1 and 13 can be found at least at the cited locations in the specification and drawings.

The present invention, as claimed in independent claim 1, provides a method for forming a semiconductor device comprising forming a 3-dimensional (3D) pattern in a substrate and depositing at least one material over the substrate in accordance with

desired characteristics of the semiconductor device. (See, e.g., specification at page 5, lines 20-25; Figure 1; reference numbers 110 and 120).

The present invention, as claimed in independent claim 13, provides a system for forming a semiconductor device comprising means for forming a 3-dimensional (3D) pattern in a substrate and means for depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device. (See, e.g., specification at page 6, lines 19 – page 7 line 5; Figures 3 and 4; reference numbers 310, 320, 330, 340, 405, 410 and 415).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

i. **Claims 1 and 13 stand rejected under 35 U.S.C. §102(b) as being anticipated by Dai (USPN 5,877,076).**

ii. **Claims 3, 14 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dai (USPN 5,877,076) in view of Taussig et al (USPN 6,861,365).**

ARGUMENT

I. The Applicable Law

35 U.S.C. §102

We respectfully remind the Examiner that in order to anticipate a claim, US Patent 5,877,076 to Dai (hereinafter *Dai*) must teach **every element of the claim** and ***"the identical invention must be shown in as complete detail as contained in the ... claim."*** *MPEP 2131* citing *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989) (emphasis added).

35 U.S.C. §103

The standard for making an obviousness rejection is currently set forth in MPEP 706.02(j):

> To establish a *prima facie* case of obviousness, *three basic criteria must be met*. **First**, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. **Second**, there must be a reasonable expectation of success. **Finally**, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The ***teaching or suggestion*** to make the claimed combination **and** the ***reasonable expectation of success*** **must** ***both be found in the prior art,*** **and not** ***based on applicant's disclosure.*** (emphasis and formatting added) MPEP § 2143, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)
>
> The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a ***convincing line of reasoning*** as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). (emphasis added).

See also, KSR International Co. v. Teleflex Inc., No. 04-1350, 550 U.S. __ (2007).

As noted above, the PTO has the burden of establishing a prima facie case of obviousness under 35 USC §103. The Patent Office must show that some reason to combine the elements with some rational underpinning that would lead an individual of ordinary skill in the art to combine the relevant teachings of the references. *KSR International Co. v. Teleflex Inc.*, No. 04-1350, 550 U.S. __ (2007); *In re Fine*, 837 F.2d 1071, 1074 (Fed. Cir. 1988). Therefore, a combination of relevant teachings alone is insufficient grounds to establish obviousness, absent some reason for one of ordinary skill in the art to do so. *Fine* at 1075. In this case, the Examiner has not pointed to any cogent, supportable reason that would lead an artisan of ordinary skill in the art to come up with the claimed invention.

Additionally, ***motivation coming from the appellant's own disclosure is not sufficient.*** Nor is it sufficient that those of ordinary skill in the art had the capability to combine the referenced structure or understood the advantages of the combination. Although an Examiner may suggest that the structure of a primary prior art reference *could* be modified in view of a secondary prior art reference to form the claimed structure, the mere fact that the prior art *could* be so modified does not make the modification obvious ***unless the prior art suggested the desirability of the modification***. *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (CAFC 1989). (Emphasis added.)

II. Rejection of 1 and 13 under 35 U.S.C. §102(b) as being anticipated by Dai (USPN 5,877,076).

The Examiner rejected Claims 1 and 13 under 35 U.S.C. §102(b) as being anticipated by *Dai*. The Appellant respectfully traverses the rejection of **Claims 1** and **13** because all of the elements of independent **Claims 1** and **13** are not taught or suggested by *Dai*, as emphasized by the recited claim elements set forth below.

> Independent **Claim 1** recites a method for forming a semiconductor device comprising:
>
> forming a 3-dimensional (3D) pattern in a substrate; and
>
> depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.
>
> Independent **Claim 13** recites a system for forming a semiconductor device comprising:
>
> means for forming a 3-dimensional (3D) pattern in a substrate; and
>
> means for depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

The Examiner states that the *Dai* reference anticipates the present invention. Appellant respectfully disagrees and asserts that ***the Dai reference does not disclose forming a 3-dimensional (3D) pattern in a substrate as recited in claims 1 and 13 of the present invention***. (Emphasis added.) *Dai* discloses a method for forming dual damascene interconnections in semiconductor chips through the use of opposite type two-layered photoresist process. A silicon substrate is provided having a composite

layer comprising a first layer of dielectric separated from a second layer of dielectric by an intervening intermediate layer of silicon nitride. Then, a layer of positive (P-type) chemical amplification resist (CAR) is deposited over the composite dielectric layer. The P-type resist is next line patterned by exposing and developing it through a dark field mask. This is followed by cross-linking the remaining P-type resist by performing a hard-bake. An opposite polarity, namely, a negative (N-type) CAR is next formed over the opposite P-type resist, and hole patterned through a clear field mask.

Because of cross-linking, the P-type resist is not affected during hole patterning of the opposite N-type resist. The hole pattern is next transferred by dry etching into the top dielectric layer and then into the intervening silicon nitride layer in the composite layer. The line pattern in the P-type CAR layer is etched into the top dielectric layer at the same time the hole pattern is transferred from the top dielectric layer into the bottom dielectric layer by the same etching process. The photoresist layers are then removed and the dual damascene structure thusly formed is filled with metal forming the line trench and hole interconnection on the semiconductor substrate.

While *Dai* discloses a substrate layer (110), the ***Dai reference does not disclose forming a 3-dimensional (3D) pattern in a substrate as recited in claims 1 and 13 of the present invention***. The Examiner asserts that *Dai* discloses forming a 3-dimensional pattern (161', 151') in a substrate. Appellant respectfully disagrees. ***The pattern(s) 161', 151' that the Examiner references are not formed in the substrate (110).*** The patterns are formed in the composite dielectric insulation layers 120, 130, 140 (see Figure 3j, Dai). Consequently, *Dai* does not teach or suggest forming a 3-dimensional (3D) pattern in a substrate as recited in claims 1 and 13 of the present invention.

Since *Dai* does not teach or suggest forming a 3-dimensional (3D) pattern in a substrate as recited in claims 1 and 13 of the present invention, the *Dai* reference does not teach or suggest each element of independent **Claims 1** and **13**. Accordingly, the rejection of **Claims 1** and **13** under **35 U.S.C. §102(b)** should be withdrawn.

III. Rejection of claims 3, 14 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dai (USPN 5,877,076) in view of Taussig et al (USPN 6,861,365).

The Appellant respectfully traverses the rejection of **Claims 3, 14** and **17** as being unpatentable over US Patent **5,877,076** to *Dia* in view of US Patent ***6,861,365*** to *Taussig et al.* **Claims 3, 14** and **17** depend from independent **Claims 1** and **13** respectively and inherit all of their limitations. Therefore, **Claims 3, 14** and **17** are also patentably distinct in light of US Patent **5,877,076** to *Dia* in view of US Patent ***6,861,365*** to *Taussig et al.* and the rejections of **Claims 3, 14** and **17** under **35 U.S.C. §103(a)** ought to now be withdrawn.

IV. Allowable Subject Matter

The Examiner has indicated that **Claims 2, 4-10, 15-16, 18-20** and **22-23** are objected to as being dependent upon a rejected base claim, but would be allowed if rewritten in independent form including all of the limitations of the base claim. Applicant appreciates Examiner's findings. In light of the above remarks concerning the lack of anticipation and failure to properly support a finding of obviousness, applicant contends that the allowability of **Claims 2, 4-10, 15-16, 18-20** and **22-23** remains unchanged, but that a re-write for independent standing is no longer necessary.

CONCLUSION

For the above reasons, Appellants respectfully submit that the cited references neither anticipate nor render obvious claims of the pending Application. The pending claims distinguish over the cited references, and therefore, Appellants respectfully submit that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-10, 13-20, 22 and 23 be allowed.

Any inquiry regarding this Response should be directed to Wendell J. Jones at Telephone No. (408) 938-0980. In addition, all correspondence should continue to be directed to the following address:

IP Administration
Legal Department, M/S 35
HEWLETT-PACKARD COMPANY
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Respectfully submitted,

Mei

By their attorney,

Wendell J. Jones

Date: June 10, 2008

/Wendell J. Jones/
Wendell J. Jones
Reg. No. 45,961

CLAIMS APPENDIX

1. (Original) A method for forming a semiconductor device comprising:

forming a 3-dimensional (3D) pattern in a substrate; and

depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

2. (Original) The method of claim 1 wherein forming the 3D pattern further comprises:

depositing a layer of material onto the substrate; imprinting a 3D pattern into the layer of material; and

transferring the 3D pattern into the substrate.

3. (Original) The method of claim 1 wherein the semiconductor device comprises a cross-point memory array.

4. (Original) The method of claim 2 wherein the semiconductor device is at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse.

5. (Original) The method of claim 2 wherein imprinting a 3D pattern into the layer of material further comprises utilizing a 3D stamping tool to create the 3D pattern.

6. (Original) The method of claim 2 wherein imprinting a 3D pattern into the layer of material further comprises utilizing a molding process to imprint the 3D pattern into the layer of material.

7. (Original) The method of claim 2 wherein the layer of material comprises a polymer material.

8. (Original) The method of claim 2 wherein the layer of material comprises a

photo-resist material.

9. (Original) The method of claim 2 wherein transferring the 3D pattern into the substrate includes:

removing a portion of the layer of material thereby exposing a portion of the substrate;

etching the exposed portion of the substrate;

removing another portion of the layer of material thereby exposing a second portion of the substrate;

etching the second portion of the substrate; and

removing a remaining portion of the layer of material.

10. (Original) The method of claim 3 wherein depositing at least one material over the substrate further comprises:

depositing two sets of conductors with a semiconductor layer there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place.

11. (Withdrawn) The method of claim 9 wherein depositing at least one material over the substrate further comprises:

depositing a first metal layer on the substrate;

applying a first planarizing polymer to the metal layer;

removing a portion of the first planarizing polymer;

utilizing the first planarizing polymer as an etch mask to etch the first metal layer thereby leaving a remaining portion of the first metal layer;

etching the substrate in a selective fashion; and

removing the first planarizing polymer.

12. (Withdrawn) The method of claim 11 wherein depositing at least one material over the substrate further comprises:

depositing a second metal layer on the remaining portion of the first metal layer;

applying a second planarizing polymer to the second metal layer;

removing a portion of the second planarizing polymer;

utilizing the second planarizing polymer as an etch mask to etch the second metal layer; and

removing the second planarizing polymer.

13. (Original) A system for forming a semiconductor device comprising:

means for forming a pattern in a substrate wherein the pattern is 3-dimensional; and

means for depositing at least one semiconductor material over the substrate in accordance with desired characteristics of the semiconductor device.

14. (Original) The system of claim 13 wherein the semiconductor device comprises a cross-point memory array.

15. (Original) The system of claim 13 wherein the means for forming the pattern further comprises:

means for depositing a layer of material onto the substrate;

means for imprinting a 3D pattern onto the layer of material; and

means for transferring the 3D pattern into the substrate.

16. (Original) The system of claim 14 wherein the means for depositing at least one semiconductor material over the substrate further comprises:

means for depositing two sets of conductors with a semiconductor layer there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place.

17. (Original) The system of claim 14 wherein the semiconductor device is at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse.

18. (Original) The system of claim 15 wherein the means for imprinting a 3D pattern into the layer of material further comprises means for implementing a molding process to imprint the 3D pattern into the layer of material.

19. (Original) The system of claim 15 wherein the means for transferring the 3D pattern into the substrate includes:

means for removing a portion of the layer of material thereby exposing a portion of the substrate;

means for etching the exposed portion of the substrate;

means for removing another portion of the layer of material thereby exposing a second portion of the substrate;

means for etching the second portion of the substrate; and

means for removing a remaining portion of the layer of material.

20. (Original) The system of claim 15 wherein the means for imprinting a 3D pattern onto the layer of material further comprises means for utilizing a 3D stamping tool to create the 3D pattern.

21. (Withdrawn) The system of claim 15 wherein the means for depositing at least one semiconductor material over the substrate further comprises:

means for depositing a first metal layer;

means for applying a planarizing polymer to the first metal layer;

means for removing a portion of the planarizing polymer;

means for utilizing the planarizing polymer as an etch mask to etch the first metal layer thereby leaving a remaining portion of the first metal layer;

means for etching the substrate in a selective fashion; and

means for removing the planarizing polymer.

22. (Original) The system of claim 15 wherein the layer of material comprises a

polymer material.

23. (Original) The system of claim 15 wherein the layer of material comprises a photo-resist material.

24. (Withdrawn) The system of claim 21 wherein the means for depositing at least one semiconductor material over the substrate further comprises:

means for depositing a second metal layer on the remaining portion of the first metal layer;

means for applying a second planarizing polymer to the second metal layer;

means for removing a portion of the second planarizing polymer;

means for utilizing the second planarizing polymer as an etch mask to etch the second metal layer; and

means for removing the second planarizing polymer.

25. (Withdrawn) A method for forming a semiconductor device comprising:

forming a 3-dimensional (3D) pattern in a substrate;

depositing a first metal layer on the substrate;

applying a first planarizing polymer to the metal layer;

removing a portion of the first planarizing polymer;

utilizing the first planarizing polymer as an etch mask to etch the first metal layer thereby leaving a remaining portion of the first metal layer;

etching the substrate in a selective fashion; and removing the first planarizing polymer.

26. (Withdrawn) The method of claim 25 wherein the semiconductor device comprises a cross-point memory array.

27. (Withdrawn) The method of claim 25 further comprising:

depositing a second metal layer on the remaining portion of the first metal layer;

applying a second planarizing polymer to the second metal layer;

removing a portion of the second planarizing polymer;

utilizing the second planarizing polymer as an etch mask to etch the second metal layer; and

removing the second planarizing polymer.

28. (Withdrawn) A semiconductor device comprising:

a substrate wherein the substrate comprises a 3D pattern formed therein;

at least one material deposited thereon in accordance with desired characteristics of the semiconductor device.

29. (Withdrawn) The semiconductor device of claim 28 wherein the 3D pattern is formed with the following process:

depositing a layer of material onto the substrate;

imprinting a 3D pattern into the layer of material; and

transferring the 3D pattern into the substrate.

30. (Withdrawn) The semiconductor device of claim 29 wherein transferring the 3D pattern into the substrate includes:

removing a portion of the layer of material thereby exposing a portion of the substrate;

etching the exposed portion of the substrate;

removing another portion of the layer of material thereby exposing a second portion of the substrate;

etching the second portion of the substrate; and

removing a remaining portion of the layer of material.

Appeal Brief to the Board of Patent Appeals and Interferences
Appellant: Mei
Serial No.: 10/769,127
Filed: January 30, 2004
Docket No.: 200209576-1
Title: FORMING A SEMICONDUCTOR DEVICE

EVIDENCE APPENDIX

None.

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RELATED PROCEEDINGS APPENDIX

None.